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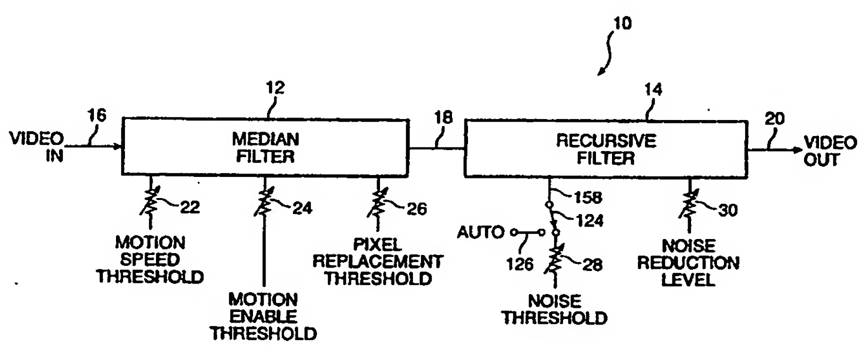

(57) Abstract

According to a presently preferred embodiment of the invention, image enhancement apparatus for digital video images comprises a two-stage filter (12) comprising a median filter (12) and recursive filter (14). The median filter operates in one, two, and three dimensions wherein the cluster of pixels framing the center pixel are ranked, and the median value of the pixel cluster is chosen as the correct pixel value. The pixel cluster configuration is selectable, as are the planes where the pixels are located. Multiple weights may be given to the appropriate median filter inputs. A motion detector (78) is used to prevent replacement of each pixel by its pixel cluster median value when there is excessive motion. Finally an adjustable pixel-replacement threshold is defined. Each pixel must deviate from its median value before it is replaced by that value. In the presence of rapid motion in the picture, the operation of the medial filter is reduced or halted by a properly derived motion signal according to the present invention, thus preventing motion artifacts from occurring.

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SPECIFICATION

THREE-DIMENSIONAL MEDIAN AND RECURSIVE FILTERING FOR VIDEO IMAGE ENHANCEMENT

BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates to video image enhancement. More particularly, the present invention relates to digital electronic noise-reduction techniques for high-quality video image improvement.

2. The Prior Art

It is known in the prior art to use median filters and temporal-recursive filters as effective methods for video image noise reduction. These two filtering methods may be used individually, or in combination, for better overall performance.

Median filtering is also known as rank-value filtering or rank-order filtering. By any name it is a well-known image-processing technique that combines pixels in a non-linear manner, and is particularly effective against impulsive noise and film grain and dirt when a three-dimensional pixel cluster is employed. Because median filters operate on discrete pixel values, the video must be in digitized form by nature.

Recursive filtering combines pixels spaced by exactly one video frame in an algebraic manner through controlled feedback, and is effective at reducing random noise by decreasing the temporal resolution in the noisy areas of the image while always preserving the horizontal and vertical resolution. Recursive filtering is not restricted to digital video images by nature, although providing an exact one-frame recursion delay is difficult by any other means. Median filtering coupled with recursive filtering gives better overall noise-reduction performance than either method when used independently.

The use of median and recursive filters for image processing has been reported in the literature. United States Patent No. 4,058,836 to Drewery et al, teaches noise reduction by

means of a recursive filter controlled by a motion detector. G. Wischermann, "Median Filtering of Video Signals - A Powerful Alternative", SMPTE Journal July 1991, discloses the benefit of the use of median filters in video images. A. Christopher et al., "A VLSI Median Filter for Impulse Noise Elimination in Composite or Component TV Signals", IEEE Transactions on Consumer Electronics, Vol. 34, No. 1, Feb. 1988, discloses the use of a pixel-replacement threshold to reduce median filter artifacts. United States Patent No. 4,928,258 to May, teaches the use of a median filter in two and three dimensions with multiple weighted inputs, also known as multiple-input counting. British Patent Application No. GB 2 139 039 A to Storey, teaches electrical means for detecting the presence of film dirt in video signals.

In addition, at least one commercially available noise reduction system employs both median and recursive filtering. Broadcast Television Systems, Inc. of Salt Lake City Utah offers a model MNR9 Median noise reducer which employs selectable pixel clustering. The BTS product is prone to strong motion artifacts.

The state of the art in video image improvement using either median filtering or recursive filtering falls short of providing sufficient performance, closely related to noise reduction effectiveness, with acceptable motion artifacts and resolution loss in pictures with high motion content. In order of discovery, the Drewery teaching of recursive-only noise reduction is very fundamental, but the system performance reaches its limit for images with average signal-to-noise ratio (SNR) before producing noticeable motion artifacts. The concept of video random and impulsive noise reduction by means of a median filter is shown by Wischermann. While in this application the performance is quite good with still pictures, small motion in the picture produces motion artifacts and loss of video resolution. Christopher et al. implemented a manual pixel-replacement threshold logic at the output of a two-dimensional median filter in an attempt to minimize the blurring artifacts, but use of this threshold alone compromises the median filter effectiveness. May's invention is not geared toward high-quality video images, hence motion artifacts and

picture resolution loss are more acc ptable in his application. The Storey disclosur represents the state of the art in motion detection, although there is no suggestion to employ it in combination with a median filter.

It is an object of the invention to provide an apparatus and method for improving digital video images by removing noise and film grain and dirt through the use of digital electronic filtering, while creating a minimum of filtering artifacts.

BRIEF DESCRIPTION OF THE INVENTION

According to a presently preferred embodiment of the invention, image enhancement apparatus for digital video images comprises a two-stage filter. The first stage of image improvement consists of a median filter selectively operable in one, two, and three dimensions (horizontal, vertical, and temporal, respectively) wherein the cluster of pix ls framing the center pixel are ranked, and the median value of the pixel cluster is chosen as the correct pixel value. In absence of video image motion, this process is very effective in locating the most likely pixel value that belongs in the center of the cluster even in presence of noise.

According to the present invention, the pixel cluster configuration of the median filter is selectable, as are the planes where the pixels are located. Multiple weights may be given to the appropriate median filter inputs. A motion detector is used to prevent replacement of each pixel by its pixel cluster median value when there is excessive motion. In addition, an adjustable pixel-replacement threshold is defined, and each pixel must deviate from its median value by a threshold amount before it is replaced by that value. In the presence of rapid motion in the picture, motion artifacts are readily generated in prior-art median filter based systems because the median filter is unable to locate the correct pixel value. The picture is thereby rendered unnatural. According to the present invention, the operation of the median filter is reduced or halted by a properly derived motion signal according to the present invention, thus preventing motion artifacts from occurring.

The second stage of image improvement makes use of the conventional recursiv filter as taught by Drewery, operating in the time domain. This process is particularly effective in averaging co-sited pixels temporally spaced and its effectiveness is enhanced when preceded by a stage containing the median filter.

In the case of video signals obtained from film by a telecine, the invention is particularly useful in removing film grain scratches and dirt as well as noise in the video. The same embodiment is also most effective in handling very noisy video images containing impulsive noise. The high level of video quality improvement is made possible by the use of three-dimensional median and recursive filters operating in tandem. Both median and recursive filters are optimally controlled through the use of motion detectors whose threshold settings are coupled to the main control of noise reduction to maximize the level of image improvement and minimize motion artifacts.

By cascading two stages of independently operating noise-reduction circuits utilizing different principles of noise reduction with the aid of motion-detection processing and control, it is possible to obtain the best results of noise reduction, impulsive noise elimination, film grain reduction, removal or reduction of film dirt and scratches and stabilization of picture jerkiness with a minimum of motion artifacts and loss of video resolution.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a presently preferred embodiment of a digital image improvement system according to the present invention.

FIG. 2 is a block diagram of the computation core of the median filter of the digital image improvement system of the present invention.

FIGS. 3a-3o are representations of various preferred median-filter cluster configurations according to the present invention.

FIG. 4 is a block diagram of a median-filter motion processor for use in the digital

image improvement system of FIG. 1.

FIG. 5 is a block diagram of a presently preferred embodiment of the selector circuit of FIG. 2.

FIG. 6 is a block diagram of a recursive filter for use in a presently preferred embodiment of the present invention.

FIG. 7 is a diagram illustrating a preferred transfer function for the non-linear transfer block of the recursive filter of the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons.

Referring first to FIG. 1, a block diagram of a presently preferred embodiment of a digital image improvement system 10 according to the present invention is presented. The digital image improvement system 10 of the present invention comprises two main subcomponents, median filter 12 and recursive filter 14. According to the present invention, these two subcomponents are arranged in a cascade configuration. Thus a video input bus 16 presents a stream of video pixels in real time to median filter 12. the output of median filter 12 is presented as a stream of video pixels in real time on bus 18 to recursive filter 14, and the output of recursive filter 14 on bus 20 comprises the output of digital image improvement system 10.

As may be seen from FIG. 1, median filter 12 has user-selectable motion speed threshold control 22, motion enable threshold control 24, and pixel replacement threshold control 26. Recursive filter 14 has user-selectable noise threshold control 28 and noise reduction level control 30. These controls will be more fully explained herein with respect to median filter 12 and recursive filter 14.

Referring now to FIG. 2, median filter 12 is shown in more detail and is seen to

incorporate novel features which give it additional functionality representing an improvement over the prior art.

Median filter 12 takes a multibit digital video signal from input bus 16 and passes it through delay elements 32, 34, 36, and 38. Delay elements 32 and 38 delay the video pixels by one frame minus one horizontal line, such that, at any given time, the pixel present at their outputs are from the same horizontal position one line above the pixel present at their inputs, but from the previous frame. Delay elements 34 and 36 each delay the video signal one horizontal line such that the pixel present at their outputs at any given time is from the same horizontal position one line above the pixel present at their inputs from the same frame. As will be appreciated by those of ordinary skill in the art, delay elements 32, 34, 36, and 38 may comprise conventional digital delay elements, such as serial shift register chains or the like.

The overall effects of delay elements 32, 34, 36, and 38 are such that if the current pixel of interest is present at node 40 at the output of delay element 34, the pixels present at nodes 42 and 44, the outputs of delay elements 32 and 36, respectively, will be the pixels from the same horizontal positions in the lines immediately below and above the pixel of interest. Further, the pixels present at nodes 46 and 48,the input of delay element 32, will be the pixels from the succeeding and preceding frames, respectively, occupying the same position in the those frames as the pixel of interest.

The heart of median filter 12 is rank-value filter element 50, which, according to a presently preferred embodiment of the invention, may be a L64220 rank-value filter integrated circuit, available from LSI Logic Corp., of Milpitas, California. The data sheet for the L64220 rank-filter integrated circuit is expressly incorporated by reference herein. Rank-value filter element 50 includes a rank-selector circuit portion 52 which takes inputs from a plurality of shift registers 54, 56, 58, 60, 62, 64, 66, and 68. The function of rank-selector circuit 52 is to select the median value from among the inputs presented.

Shift registers 54, 56, 58, 60, 62, 64, 66, and 68 are eight-bit serial shift registers in the L64220 integrated circuit, but those of ordinary skill in the art will recognize that other configurations are possible. By employing these serial shift registers, the present invention can define the median value of the pixel of interest in terms of the pixels to its immediate left and right, as well as pixels immediately above and below (from delay elements 34 and 36).

Rank-value filter element 52 is controlled by control unit 70, which selects which pixel values stored in the shift registers 54, 56, 58, 60, 62, 64, 66, and 68 are used in the median value determination. As disclosed in the L64220 Data Sheet from LSI Logic, expressly incorporated by reference herein, any pixel element in the shift registers 54, 56, 58, 60, 62, 64, 66, and 68 can be masked such that the pixel cluster used to compute the median value is selectable. Loading of the masking registers in the L64220 integrated circuit is easily and routinely accomplished by employing the address, clock, and write-enable inputs provided. Those of ordinary skill in the art will recognize that a microcontroller could easily be employed to provide selectable clusters by controlling the address, clock, and write-enable inputs to load preselected patterns into the mask registers in the control section 70 of rank-value filter element 50.

From an examination of FIG. 2, those of ordinary skill in the art will readily recognize that the pixels from nodes 40, 46, and 48 are each presented to two shift registers at the same time. Thus, the pixels present at node 46 are presented to shift registers 54 and 56, the pixels present at node 40 are presented to shift registers 60 and 62, and the pixels present at node 48 are presented to shift registers 66 and 68. This arrangement allows the possibility of double-counting these pixel values in the median value computation.

Referring now to FIGS. 3a-3o, diagrammatic representations of the various pixel clusters from which the median value can be calculated are shown according to a presently preferred embodiment of the invention. FIGS. 3a-3o show combinations of both positional

and temporal clustering, using left, right, horizonal, vertical, and diagonal nearest neighbors in the positional domain, and corresponding past and next frame pixels and their immediate left, right, horizonal, and vertical neighbors in the temporal domain. From FIGS. 3a-3o, those of ordinary skill in the art can see the cluster geometries made possible by use of the delay elements 32, 34, 36, and 38. Each pixel position is represented by a circle and the double-counted pixels are shown as double circles. The present embodiment can accept any pixel cluster covering the present frame with 0, 1 or 2 votes, the preceding and following frames both with 0, 1 or 2 votes, and the lines above and below each with 0 or 1 votes. According to the presently preferred embodiment of the invention, only the corresponding pixels in the immediately preceding and succeeding frames may be double-counted by having 2 votes, since these pixels introduce the least degradation of spatial resolution, but those of ordinary skill in the art will realize that other configurations are possible by suitably modifying the delay elements and doubling of serial shift register inputs. Each cluster configuration except for that illustrated in FIG. 3o is symmetric in each of the 3 dimensions. The configuration FIG. 3o may be used when the median filter is inactive, and a minimum overall video delay is desirable. The selection of which pixel cluster to employ may be user-selectable by means of, for example, a simple selector switch.

Referring again to FIG. 2, a compensation delay 72 is connected to node 40 in order to enable complete bypassing of median filter 12. The amount of delay provided by compensation delay 72 is such as to provide at its output the pixel value whose computed median value is simultaneously present at output 74 of rank-value filter 50. The output of compensation delay 72 and the output 74 of rank-value filter 50 are provided to selector 76. The function of selector 76 is to pass the pixel value from one of compensation delay 72 and the output 74 of rank-value filter 50 to output bus in response to a threshold select signal. The structure and operation of selector 76 will be described with reference to FIG. 5.

A motion detector circuit 78 is advantageously employed in m dian filter 12 to reduce the amount of temporal filtering so as not to introduce blurring motion artifacts in moving areas of the image which require full temporal resolution. The structure and operation of a presently preferred motion detector 78 will be described with reference to FIG. 4, to which attention is now drawn.

Referring now to FIG. 4 , it may be seen that motion detector 78 comprises two sections, motion processor 80 and global motion detector 82, both shown within dashed lines on FIG. 4. Motion processor 78 operates on the luminance portion of the digital video signal and two signals delayed by one frame each using frame delays 84 and 86, which may comprise conventional digital delay elements. As indicated on FIG. 4, the output of frame delay 86 is a pixel from frame A, the output of frame delay 84 is the corresponding pixel from frame B, and the input to frame delay 84 is the corresponding pixel from frame C, where frame B is a current video frame and frames A and C are the proceeding frame and the following frame. Where there are differences in the pixel values of the corresponding pixel in frames A, B, and C, these differences could be caused by motion in the picture or, for images originated from film, from dirt and or scratches on the film. It is therefore imperative to derive motion information from the video itself if the frame contains interframe motion, in order to prevent erroneous operation of the median filter which will smear the image by misinterpreting motion as noise or dirt.

Motion processor 80 derives three signals, |A-B|, |B-C|, and |A-C|, using digital subtractor circuits 88, 90, and 92, and absolute value circuits 94, 96, and 98, which may comprise ROM look-up tables, as is known in the art. The Global Motion Detector 82 operates by processing the absolute frame difference |B-C| from absolute value circuit 96. The |B-C| difference is processed through a line integrator circuit 100, comprising an accumulator active each pixel and reset each line, latch 102, line average circuit 104 which may comprise an accumulator active each line and reset each field, and minimum detect circuit 106, which may comprise a digital comparator active each line and reset each

field to compare the latest line integration value with the minimum line integration value, to determine the floor of video activity of every active video line, and the average value of motion through a frame by the Line Average circuit. The higher the motion content in the frame, the larger is the output of the line average circuit 104.

At the end of the video frame, the minimum detect and line average values are subtracted in subtractor circuit 108, and the difference is latched at each field time in latch 110. The Value stored in latch 110 is compared with a threshold value supplied on motion-speed threshold line 24 in decision logic 112 to determine if the frame is considered to contain fast motion or slow motion. According to a presently preferred embodiment of the invention, the threshold value is user-selectable, for example, under computer control as is well known in the art. The fast-motion/slow-motion determination at the output of decision logic 112 is a binary on/off decision.

In the Motion Processor block, three interframe comparisons of temporally co-sited pixels, |A-B|, |B-C|, and |A-C| are made in subtractor circuits 88, 90, and 92 and absolute value circuits 94, 96, and 98. According to a presently preferred embodiment of the invention, it has been determined that the larger of the first two comparison levels is the better representation of motion for fast-moving motion content. This selection is made by larger-value select circuit 114, which may comprise a digital-word comparator. For slow-moving images, the |A-C| comparison is best. Data select circuit 116, which may comprise a digital multiplexer, is used to select the output representing fast or slow motion depending on the output of decision logic 112.

The most suitable motion signal selected by data select circuit 116 is subsequently filtered in two dimensions (horizontally and vertically) by 2D filter circuit 118 to enhance the signal-to-noise ratio of the motion signal. 2D filter circuit 118 may preferably comprise a horizontal filter of seven points and a vertical filter of three points, although other configurations are possible. If the selected and filtered signal is above the motion-enable threshold 24, decision logic 120 will disable the operation of the median filter in a

binary on/off fashion at its enable input 122 (FIG. 2). The threshold setting of decision logic circuit 120 is user-adjustable by loading a selected threshold value into a register inside decision logic circuit 120, for example, under computer control as is well known in the art.

Pixel-replacement Threshold Logic selector 76 (FIG. 2) compares the median filter output to the corresponding pixel at the center of the pixel cluster and, if the difference is above the threshold value 26 set by the user, the median value is selected. Referring now to FIG. 5, the structure and operation of selector 76 will be described. The comparison of the median filter output and the central pixel value is made in subtractor circuit 150 and absolute-value circuit 152. Decision logic 154, which may comprise a digital-word comparator, decides if the compared value exceeds pixel replacement threshold 26 and issues a binary on/off output in response. Data selector circuit 156, which may comprise a multiplexer, selects either the computed median or the central pixel value for ultimate median filter output. The threshold settings for decision logic 152 are adjustable by user control, for example, under computer control as is well known in the art.

FIG. 6 is a block diagram of recursive filter 14 according to a presently preferred embodiment of the invention. The operation of recursive filter 14 is controlled by the noise threshold adjustment 28 and by the noise reduction level, adjustment 30, in the Manual Threshold mode. According to a presently preferred embodiment of the invention, recursive filter 14 may be a filter such as the one set forth in United States Patent No. 4,058,836, expressly incorporated herein by reference.

According to a presently preferred embodiment of the invention, an automatic mode of operation of recursive filter 14 is provided wherein the noise threshold adjustment is replaced by the Global Motion Detector level, updated every frame instant. This is illustrated symbolically by switch 124, which is switchable to an automatic operating node comprising the output of global motion detector 82 at automatic node 126. Switch 124 thus provides either a manual user-adjustable nois threshold control or an automatically

determined noise threshold control at point 158. FIG. 6 is a block diagram illustrating a recursive filter similar to the one disclosed in United States Patent No. 4,058,836. Vid o input is provided to one input of subtraction circuit 160. The output of subtraction circuit 160 is presented to the input of low pass filter 162, which is configured to smooth the difference signal as disclosed in United States Patent No. 4,058,836. The output of subtractor 160 is also presented to compensating delay 164, which compensates for the delay through low pass filter 162. The output of compensating delay 164 is presented to one input of multiplier 166. The other input of multiplier 166 is supplied by non-linear transfer block 168. Non-linear transfer block 168 is preferably configured to produce an output signal which is a function of input signals noise threshold 158 and noise reduction level 30 which has a transfer characteristic as shown in the graph of FIG. 7. The inputs 158 and 30 select an operating curve above which detected motion will not permit noise reduction, in order to prevent motion artifacts. As will be appreciated by those of ordinary skill in the art, non-linear transfer block 168 may be configured from a ROM lookup table. An example of a suitable ROM lookup table is provided in Appendix I.

The output of multiplier 166 is presented to one input of adder 170. The output of adder 170 forms the video output of the recursive filter. It also serves as a feedback point and is connected to frame delay 172, which introduces a delay of one frame. The output of frame delay 170 is presented to the other input of subtractor 160, as well as to the input of delay 174, which matches the delay produced by delay 164. Other than the function of non-linear transfer block 168, the operation of recursive filter 14 is disclosed in United States Patent No. 4,058,836.

A set of schematic diagrams for the circuitry which implements an actual embodiment of the invention is filed herewith as Appendix I. Specifications for the programmable devices shown thereon, is filed herewith as Appendix II. The program-control source code for an Intel 8031 microcontroller which accepts the user commands and interfaces to the system bus of the actual embodiment of the present invention described in

Appendices I and II is filed herewith as Appendix III. These diagrams and other information, which describe an actual working embodiment of the present invention, are expressly incorporated herein by reference.

Those of ordinary skill in the art will recognize that the settings for the various threshold values specified herein are somewhat subjective. The possibilities of combinations of dirt, noise, and motion in video sequences are virtually infinite and thus the threshold settings at any moment may depend on the particular video material being viewed.

While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

What is Claimed is:

1. Apparatus for enhancement of digital video images, said apparatus connectable to a source of digital video signals operating at a video pixel rate and comprising:

a median filter including storage means for temporarily storing digital data to present simultaneously data representing pixels from a current video frame, a most recent video frame, and a next video frame;

user-selectable data cluster selection means associated with said median filter and operating on each pixel in said current video frame, for identifying one of a plurality of clusters of digital data as a selected cluster from digital data stored in one or more of said current video frame, said most recent video frame, and said next video frame, each of said clusters comprising digital data representing said each pixel and ones of said pixels which are chosen from positional and temporal neighbors of the one of said each pixels being operated on, wherein at least one of said digital data may be weighted more than once, and for presenting said clusters of digital data to said median filter;

motion detector means for detecting motion in a region of said current video frame containing said each pixel, and for producing a motion-sense signal proportional to the degree of motion in said region, and

first substitution means for substituting an output of said median filter for said each pixel in said current video frame only if said motion-sense signal is below a user-selected threshold.

2. The apparatus of claim 1, further including:

first means for generating, for each pixel, a deviation threshold signal if said each pixel deviates from the median value of said selected cluster by at least a selected threshold, said selected threshold being adjustable by a user;

second substitution means for substituting an output of said median filter for said each pixel in said current video frame in response to said deviation threshold signal.

3. The apparatus of claim 1, wherein said plurality of clusters are chosen from the group including:

(1) said each pixel weighted twice, its upper and lower nearest neighbors, each weighted once, and its corresponding pixels in said most recent video frame and said next video frame, each weighted twice;

(2) said each pixel weighted twice, its left and right nearest neighbors, each weighted once, and its corresponding pixels in said most recent video frame and said next video frame, each weighted twice;

(3) said each pixel weighted twice, its upper, lower, left, and right nearest neighbors, each weighted once, and its corresponding pixels in said most recent video frame and said next video frame, each weighted twice;

(4) said each pixel weighted twice, its four diagonal nearest neighbors, each weighted once, and its corresponding pixels in said most recent video frame and said next video frame, each weighted twice;

(5) said each pixel weighted twice, its upper, lower, left, and right nearest neighbors, each weighted once, its corresponding pixels in said most recent video frame and said next video frame, each weighted twice, and their left and right nearest neighbors, each weighted once.

4. The apparatus of claim 1, further including a recursive filter having an input connected to said output of said median filter.

5. The apparatus of claim 4, wherein said recursive filter includes:

noise threshold setting means;

noise reduction level control means;

motion detector means for detecting motion in a region of said current video

frame containing said each pixel, and for producing a motion-sense signal proportional to the degree of motion in said region; and

recursion control means, responsive to said motion-sense signal, said noise threshold setting means, and said noise reduction level control means, for controlling the magnitude of recursion produced by said filter.

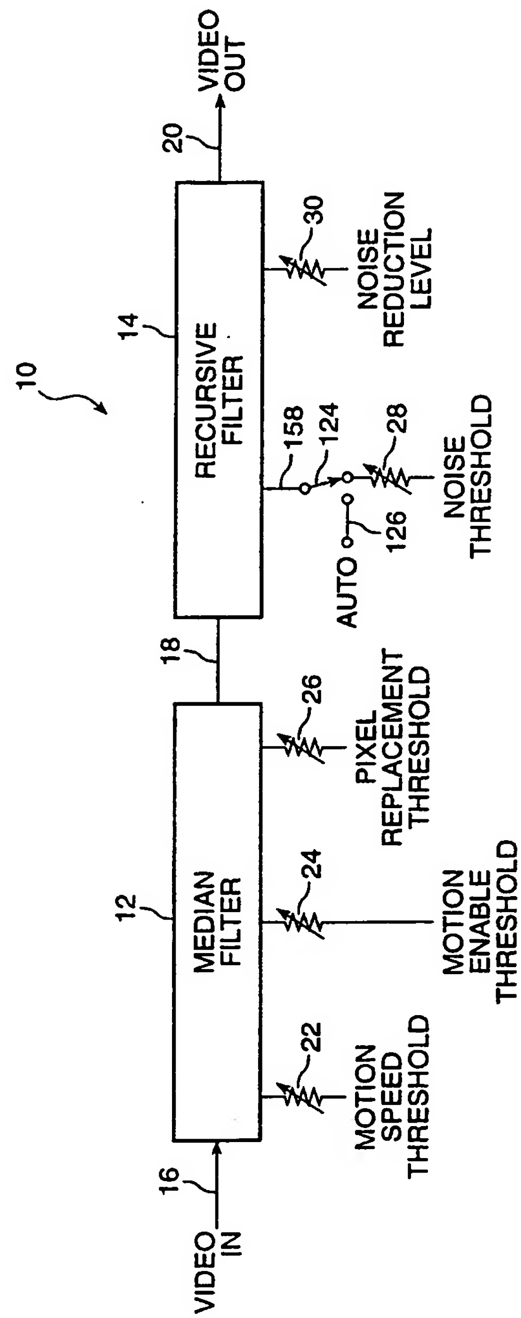

VIDEO IN
16
MEDIAN FILTER
12
MOTION SPEED THRESHOLD
22
MOTION ENABLE THRESHOLD
24
PIXEL REPLACEMENT THRESHOLD
26
18
RECURSIVE FILTER
14
10
AUTO
126
124
158
28
NOISE THRESHOLD
NOISE REDUCTION LEVEL
30
20
VIDEO OUT

FIG. 1

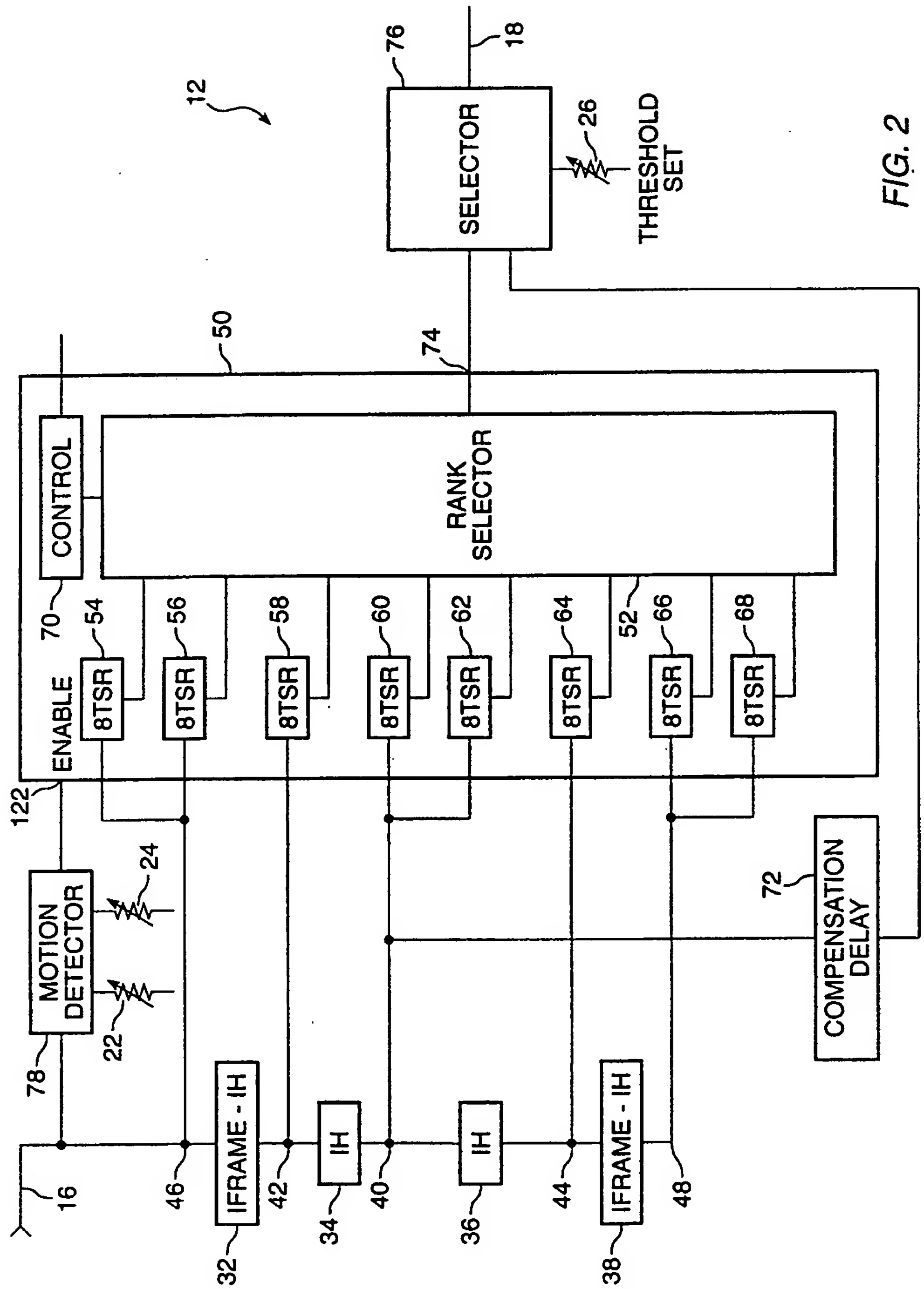

12
SELECTOR
76
18
26
THRESHOLD SET
50
74
CONTROL
RANK SELECTOR
70
ENABLE
8TSR
54
56
58
60
62
64
52
66
68
122
MOTION DETECTOR
78
22
24
COMPENSATION DELAY
72
IFRAME - IH
IH
16
46
42
40
44
48
32
34
36
38

FIG. 2

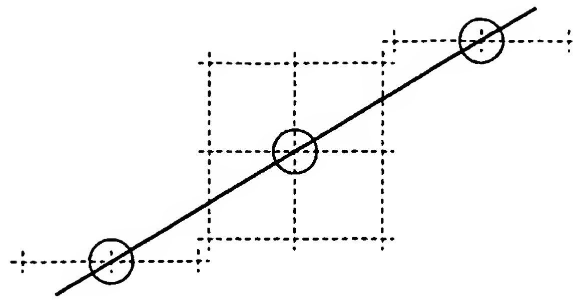


FIG. 3a

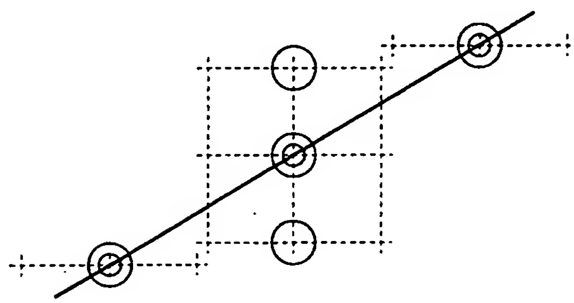


FIG. 3b

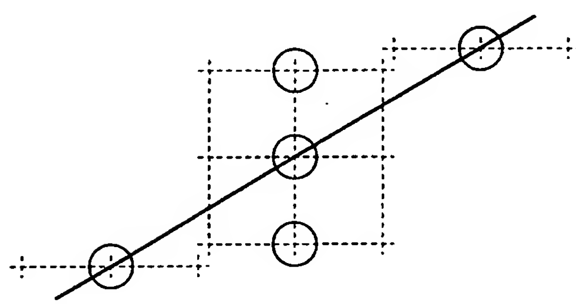


FIG. 3c

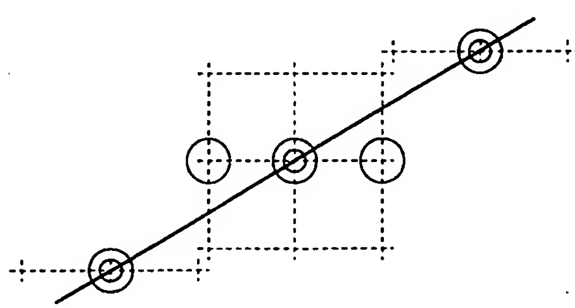


FIG. 3d

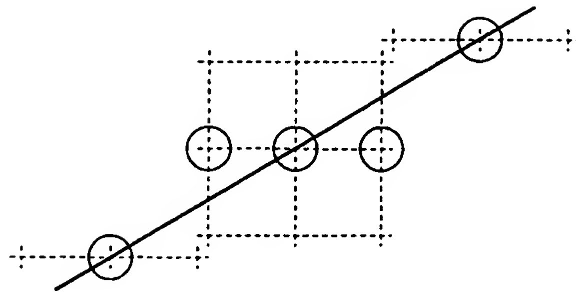


FIG. 3e

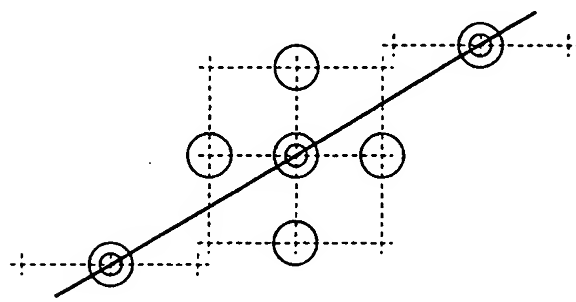


FIG. 3f

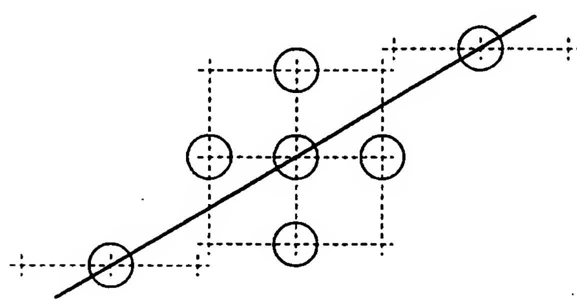


FIG. 3g

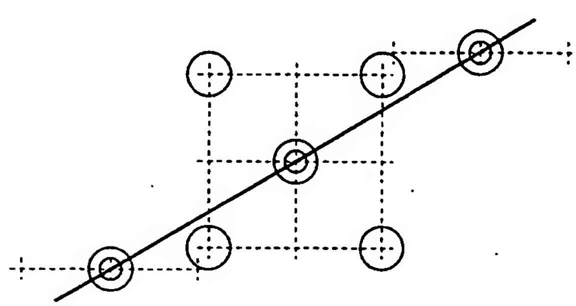


FIG. 3h

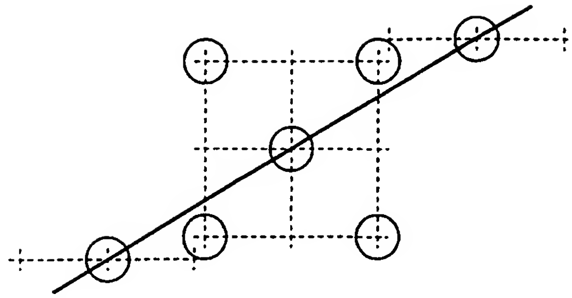


FIG. 3i

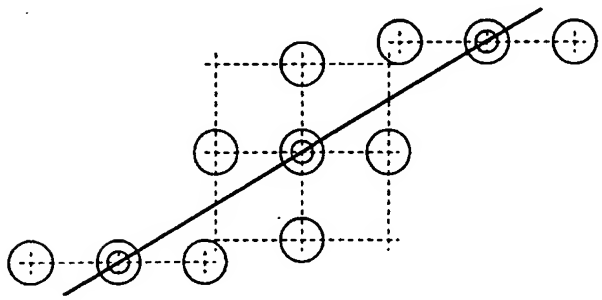


FIG. 3j

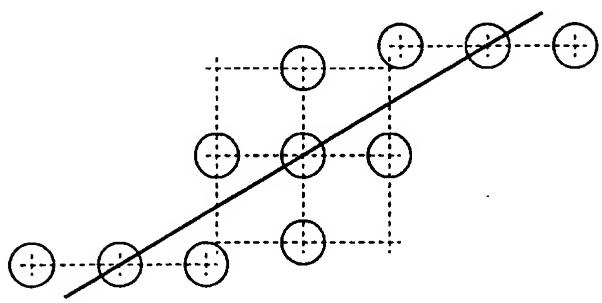


FIG. 3k

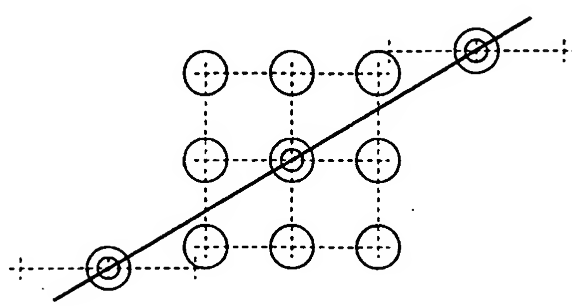


FIG. 3l

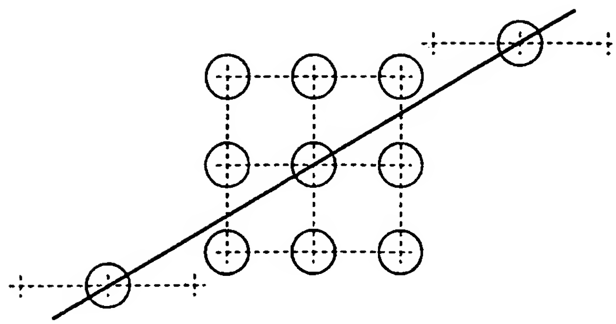


FIG. 3m

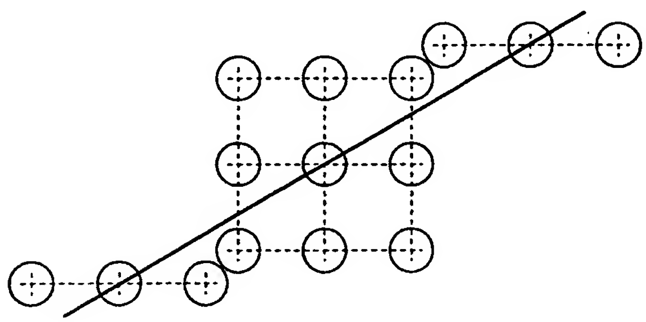


FIG. 3n

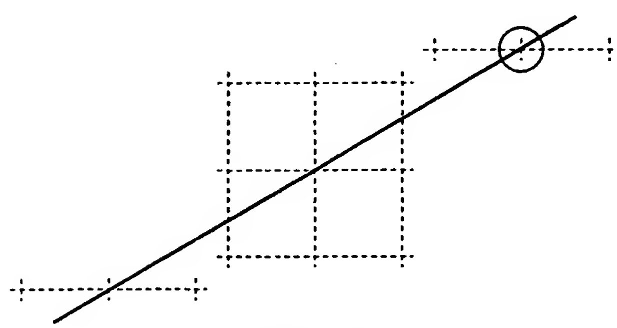
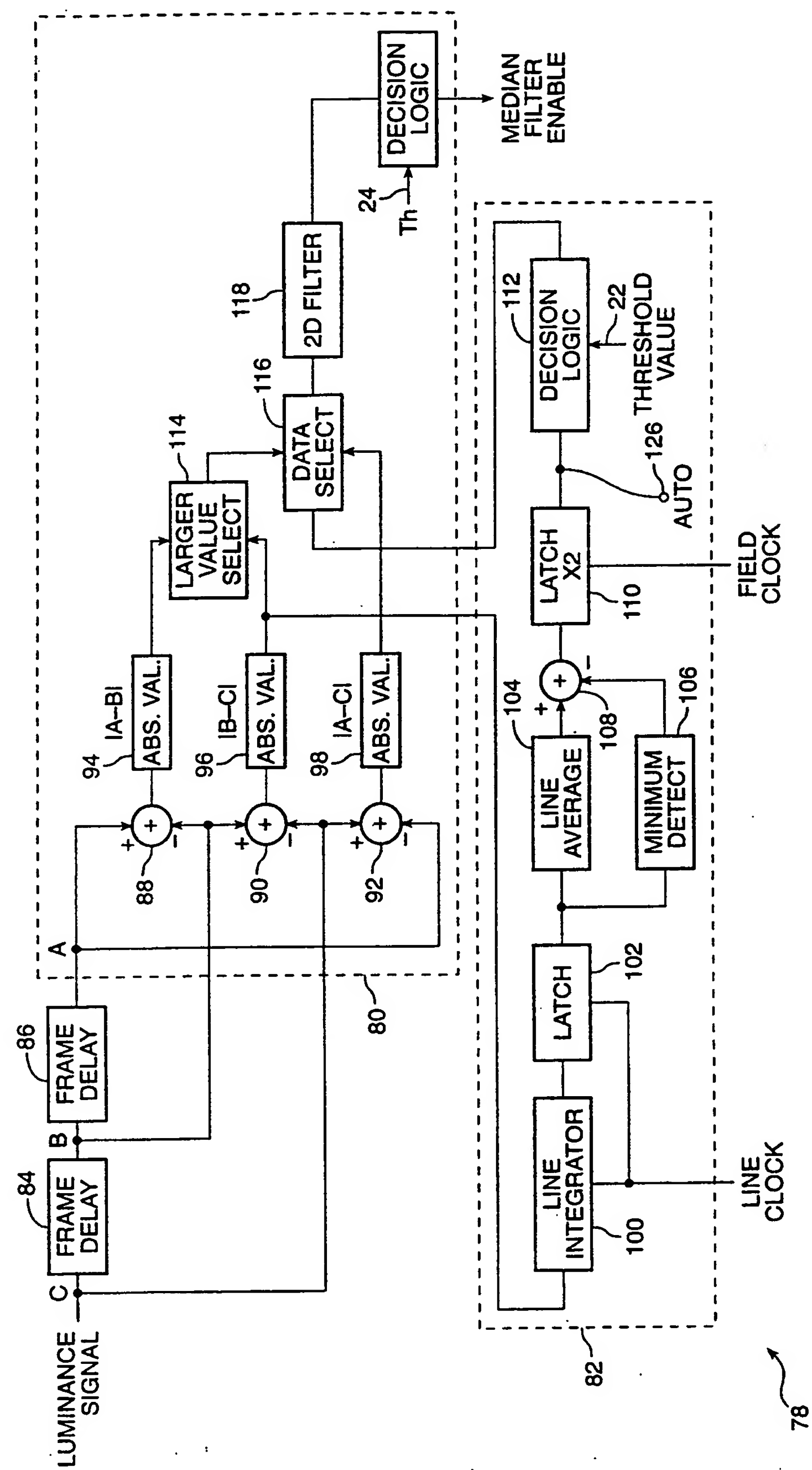


FIG. 3o



LUMINANCE SIGNAL
C
B
A
FRAME DELAY
84
FRAME DELAY
86
88
90
92
ABS. VAL.
ABS. VAL.
ABS. VAL.
94
96
98
|A–B|
|B–C|
|A–C|
LARGER VALUE SELECT
114
DATA SELECT
116
2D FILTER
118
DECISION LOGIC
24
Th
MEDIAN FILTER ENABLE
80
LINE INTEGRATOR
100
LATCH
102
LINE AVERAGE
104
MINIMUM DETECT
106
108
LATCH X2
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DECISION LOGIC
112
22
THRESHOLD VALUE
126
AUTO
FIELD CLOCK
LINE CLOCK
82
78

FIG. 4

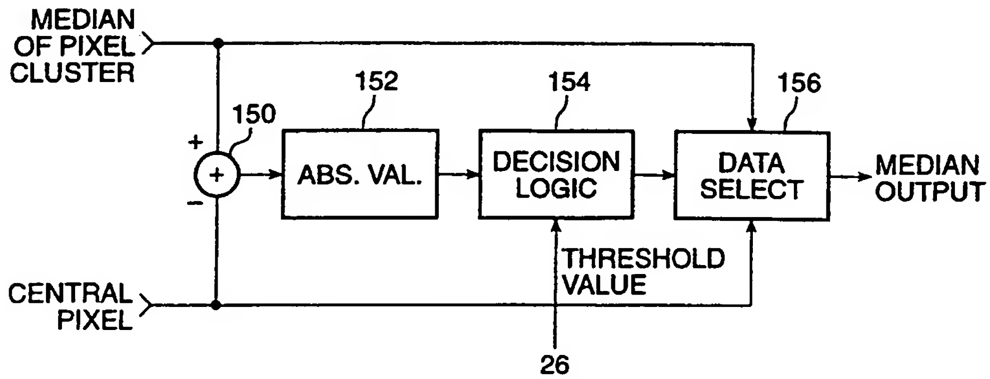

FIG. 5

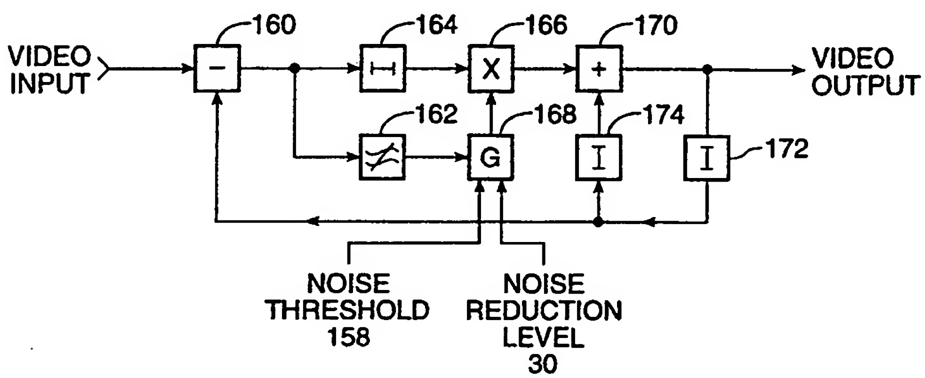

FIG. 6

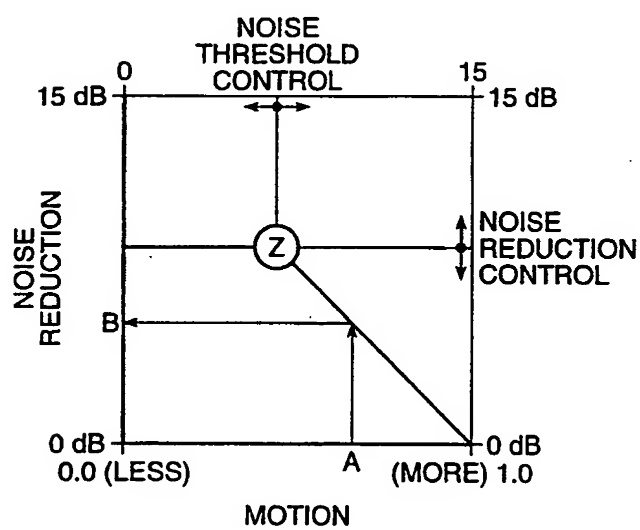

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/10298

A. CLASSIFICATION OF SUBJECT MATTER
IPC(5) :H04N 5/213
US CL :358/167, 166, 105
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 358/167, 166, 105; H04N 5/213

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	GB, A, 2 251 353 (BORER) 26 September 1988, figure 1, abstract	1
A	GB, A, 2 202 706 (WISCHERMANN) 01 July 1992, figure 3, abstract	1
A	US, A, 4,682,230 (PERLMAN ET AL.) 21 July 1987, figures 3 & 4	1
A,P	US,A, 5,161,018 (MATSUNAGA) 03 November 1992, figure 1	1,5
A	US, A, 4,928,258 (MAY) 22 May 1990, figure 16	1
A	US, A, 5,068,914 (KLEES) 26 November 1991, abstract, figure 3	3

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
07 January 1994	MAR 14 1994

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	James Jwoody Jeffrey S. Murrell
Facsimile No. NOT APPLICABLE	Telephone No. (703) 305-8155

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4,058,836 (DEWERY ET. AL.) 15 November 1977, abstract, figure 3.	1-5